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TITLE: Method and apparatus using mapped redundancy to perform multiple large block memory array repair

Detailed Description Paragraph Right (3):

Semiconductor memory device 10 additionally includes a memory redundancy circuit 20 for replacing defective locations in memory sub-arrays 14a-14p by providing substitute memory locations which may be accessed for read and write purposes in place of the defective locations. The memory redundancy circuit 20 includes two fusible address fields 22 and 23 comprising a plurality of fusible devices (not shown). The fusible address fields 22 and 23 store a number of bits indicating locations in at least one of the sub-arrays of memory array 11 for which there is redundant storage. Two redundant storage units 24 and 34 are provided for storing data in the event that there are multiple defects in the memory array 11. A compare unit 26 compares the address on address bus 12 with the information provided from the fusible address fields 22 and 23 to determine whether there is a match between the address on the bus 12 and the address stored in fusible address fields 22 or 23. The redundant circuitry 20 also includes drivers 27, coupled to the internal input/output bus 19 for communicating with that bus.

Detailed Description Paragraph Right (13):

Referring now to FIG. 3, the redundancy circuit 20 of FIG. 1 is shown to include two storage devices each having 16 rows and 128 columns. To provide column redundancy, data for Bit 0, Bit 1, Bit 2, and Bit 3 from column group 5 (corresponding to defective cell cluster 35) are stored in redundant storage unit 24. Data for Bit 0, Bit 1, Bit 2, and Bit 3 of column group 0 (corresponding to defective cell cluster 36) are stored in redundant storage unit 34. It should be noted that the 16 row and 128 column arrangement shown in FIG. 3 is merely an example layout for the redundant storage units 24 and 34, and other configurations could similarly be implemented depending on the available space in the semiconductor package.

Detailed Description Paragraph Right (44):

An additional benefit of the described arrangement is that, because the redundant storage may be totally separated from the control and addressing of the main arrays, the semiconductor memory device may be arranged such that the redundancy circuit is located in any available location on the die area. Thus, even for memory devices having a wide data path, the necessity of providing a wider package simply for providing column redundancy circuit is eliminated.